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Research Article

Nanowires: Innovative Control Growth and Applications of Silicon Crystals in 1D

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ABSTRACT

This article reviews the growth concept of silicon nanowires with an attention to semiconductor nanowires filling the gap in the knowledge from the very original work to the very recent innovative experimental work. The objectives of this article are as follows; 1-to describe the original work of epitaxial growth of semiconductor nanowires, 2-to discuss the recently emerged technique of nanoscale templating controlling the growth position of nanowires, and 3-to explore the possible technological applications of position-controlled silicon nanowires. Detailed description of the first reported successful Vapor Liquid Solid (VLS) 1-D growth of silicon crystals is presented. Bottom-up approach and the supersaturation in a three-phase system then the nucleation at the Chemical Vapor Deposition (CVD) processes are discussed with more focus on silicon. Positional assembly of nanowires using current available techniques including Nanoscale Chemical Templating (NCT) can be considered as the key part of this document for advanced applications. Several applied and conceptional methods of developing available technologies using nanowires are included, such as, Atomic Force Microscopy (AFM), Photovoltaic (PV) cells, and Metal Oxide Semiconductor Field Effect Transistors (MOSFET) are explained. The finial section of this review is devoted to the future trend in silicon nanowires research, where it is anticipated that the effort will proceed further to be implemented in daily electronic tools satisfying the demand of low wights and sizes electronics.

Keywords: Nanowires; Semiconductors; Silicon; CVD; Catalyst; PV; AFM

INTRODUCTION

The topic of semiconductor nanowires is timely developing research. Over the last few years silicon nanowires have come under intensive research due to their promising physical properties and potential as active materials in future electronic and optoelectronic applications. [1-3]. The review work on a fast developing topic is not a trivial objective, and it is even more critical with nanotechnology related subject matters. This review is focused on experimental work and progress of Silicon Nanowires (Si-NWs) technology for the past decades, with more focus on the recent few years work.

Nanowires can be grown from several materials including semiconductors, such as silicon. Nanowires made out of silicon are of particular technological importance, based on the well-known importance of Si material. Moreover, the particular advantages of nano-morphology of high ratio of surface area to volume and their related applications [4]. Any application occurs at the surface such as chemical reactions, it will speed up at a medium of high surface area [5].

Indeed, there are more features of integrating nanowires with the current available technologies, such as, Photovoltaic (PV) [2-6]. Atomic Force Microscopy (AFM) [7]. Metal Oxide Semiconductor Field Effect Transistors (MOSFET) [8-9]. Raman spectroscopy and as stands alone applications, such as sensors [9-11]. Moreover, semiconductor nanowires can be functionalized and tailored in accordance with different requirements. For example, we can dope them with particular elements in the growth stage to change electrical properties or change the growth conditions to vary their shape or size [12,13].

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MATERIALS AND METHODS

Simulation studies on the possible integration of nanowires to various device fabrication techniques is of great interest at this stage. Particularly, in building specific device structures and studying the expected I-V performance. It has been demonstrated, as an example, using a 3DS Atlas numerical quantum simulator built based on non-equilibrium green's function formalism the physical channel contraction upon nanowires integration with Field Effect Transistors (FET) [8].

There are several techniques of growing semiconductor nanowires. These fabrication methods are based on the semiconductor industrial capabilities, mainly; top-down and bottom-up approaches. Photoresist patterning on top of a silicon-on-insulator layer followed by etching silicon and creating vertical silicon columns, which is explained as top-down approach. Techniques based on the direct epitaxial growth of nanowires from a seeding material on a substrate are called bottom-up growth techniques, which is the main technique discussed in this chapter. Where the details of top-down Si-NWs fabrication approach can be found elsewhere (Figure 1) [5,14].

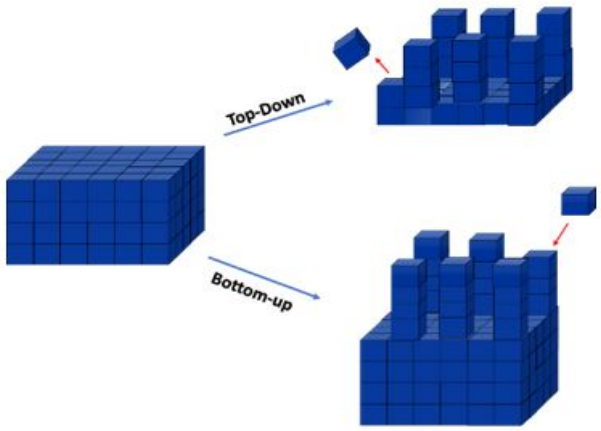

Figure 1: Schematic representation shows the original substrate, and the two main approaches of creating nanowires bottom-up and top-down approaches. Notice the building blocks of materials (atoms) are moving towards (deposition) the substrate in bottom-up process, while atoms are moving away (etching) from substrate in top-down mechanism.

Studies on Si-NWs have started with the pioneer work of Wagner and Ellis in 1965 [15-17]. The Vapor Liquid Solid (VLS) growth method uses metallic droplets or particles as a catalyst to nucleate the growth and adsorb gaseous precursors and precipitate them to permit crystal growth. The classical example is the VLS growth of Si-NWs on a Si substrate using Gold (Au) eutectic droplets. A recent work by Ramanujam has reported the growth and properties of Si-NWs. It has been reviewed various growth methods currently employed in bottom-up Si-NWs growth with special attention on Au and non-Au catalysts. Au is the most widely used catalyst for Si-NWs growth by CVD under VLS mechanism, as it offers a good size control. Indeed, there are other growths mechanisms such as Vapour Solid Solid (VSS), Solution Liquid Solid (SLS) at the Chemical Vapor Deposition (CVD) reactor, or using Molecular Beam Epitaxy (MBE), or laser ablation have been employed to address issues related to control Si-NWs, such as, diameter, aspect ratio, position. Moreover, catalyst free oxide- assisted methods have also been utilized to grow Si-NWs. Precise positioning of nanowires can be achieved by Electron Beam Lithography (EBL) [18-19].

Studying the structural properties of NWs is particularly important so that a reproducible relationship between their desired functionality and their geometrical and structural characteristics can be established. Due to the enhanced surface to volume ratio in nanowires, their properties may depend critically on their surface condition and geometrical configuration. Even nanowires made of the same material may possess dissimilar properties due to differences in their crystal phase, crystalline size, i.e., bulk substrates (3D), and nanowires (1D), or thin film or nanomembranes (2D), surface conditions, and aspect ratios, which depend on the synthesis methods and conditions used in their fabrication. Another important issue regarding the application of Si-NWs to electronics devices is how the NWs are formed at low temperatures so that the circuits are not damaged by heating. Si-NWs have been thus tried to grow at low temperatures by utilizing metal catalysts, such as Gold (Au), Aluminum (Al), whose alloys with Si have low eutectic temperatures. Generally speaking, Si-NWs have been shown to provide a promising framework for applying the bottom-up approach for the design of nanostructures for nanoscience investigations and for potential nanotechnology applications. We are certainly working in accordance with the predictions of Moore's Law, which suggests that the number of transistors in a dense integrated circuit doubles every two years [8]. Electronic devices are getting smaller and smaller, and the capabilities of these devices are becoming more leading-edge with the integration with the NWs technology.

Most studies to- date have used Au as a catalyst for Si-NWs due to the convenience of handling that arises from its resistance to oxidation. [1,4,13]. The interest in other metals for Si-NWs has arisen from the fact that Au impurities in Si act as a deep level trap decreasing the carrier mobility, lifetime, and diffusion length [20]. Avoidance of Au is therefore especially important for minority-carrier based devices such as PV devices, leading to recent efforts using Al and other nongold metals for the growth of nanowire- based photovoltaic Si structures [21]. Based on the previous, the gap in the knowledge of Si-NWs growth and applications is a comprehensive study on Si-NWs catalysed with elements such as Al which assist the growth and alloy for advanced applications. The concept of growing semiconductor nanowires is presented in the next session, along with selected resembling tabulated information of growth techniques and catalysts materials. Where semiconductor nanowires section leads us to a more a specific topic of silicon nanowires and related techniques and applications.

Epitaxial growth of semiconductor nanowires

The procedure of the bottom-up growth process of semiconductor NWs can be described as follows;

Step 1: A semiconductor substrate, which could a bulk semiconductor substrate or an epitaxial layer of a semiconductor materials on a glass.

Step 2: Thin continuous layer of few nanometers thick metal evaporated on the surface of the semiconductor epitaxial layer,

Step 3: Which segregates in isolated droplets during annealing.

Step 4: Precursor's gas flows in the Chemical Vapor Deposition (CVD) reactor, where semiconductor atoms react at the metal-droplet surfaces, depositing semiconductor vapor atoms into solution within the metal droplets.

Step 5: The catalyst droplets supersaturate, inducing precipitation of crystalline semiconductor vapor atoms upon the substrate. As precipitation occurs only at the droplet metal (liquid)–semiconductor (solid) interfaces, the semiconductor atoms crystallite in wire structures with diameters comparable to the diameter of the metal droplet.

This growth protocol has been called by Wagner and Ellis as VLS growth after the three co-existing phases: the vaporous precursors (such as Siv), liquid catalyst droplets (such as Aul) and the solid silicon substrate (Sis). Notice the possible incorporation of some of metal atoms (Au) which catalyzed the growth within the frame of the grown NW (Si-NW), as it is presented schematically in Figure 2.

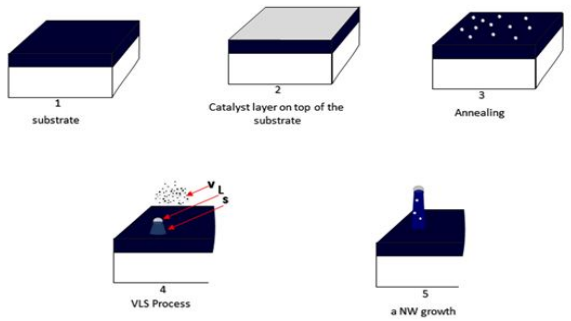

Figure 2: A schematic representation shows the sequence of the VLS process in five main steps. 1: The substrate depicted, can be bulk semiconductor materials or a relatively thin film of a semiconductor on a cheap substrate such as glass or Poly Carbonate (PC) or Poly Methyl Methyl Acrylate (PMMA) sheets, 2: catalyst thin layer, 3: catalyst after annealing where it balls up, 4: the sample was placed at the CVD reactor and allowing the precursor gas to flow, temperature reaches the eutectic and three phases co-exists, precipitation begins 5: growth continues forming NWs.

Semiconductor nanowires have been formed using various methods, as it has been summarized in Table 1. Chemical Vapor Deposition (CVD) and Molecular Beam Epitaxy (MBE) are the main growing systems for the past decade up to recent work for growing various semiconductor nanowires using several catalysts, or without catalysts (Table 1).

Table 1: Published experimental research articles of semiconductor nanowires including the techniques and the catalysts. The included representative studies of some pioneer experimental work in the very recent years (2021 and 2020), with inclusion of some work of the previous decade, would present a general view of work on semiconductor nanowires. Among semiconductor materials, this study focuses on Si-NWs which are epitaxially grown in the CVD reactor using VLS bottom-up approach.

Semiconductor materials	Growth techniques	Catalyst	References
TiO_2/In_2O_3	Electron Beam Evaporation	catalytic free glancing angle deposition technique	[22] Guney et al. 2021
GaAs	Metal–organic chemical vapor deposition (MOCVD). a Vapor Liquid Solid (VLS) mechanism	Au	[23] Zeng et al. 2021[3] Ziyuan et al. 2020
SnO_2 nanowires	A solvothermal process	Pd	[24] Lu et al. 2021
p-type α-Bi_2O_3	Vapor Liquid Solid (VLS)	different catalysts (Au, Pt and Cu) as seed layers but the highest aspect ratio was obtained using Au	[25] Moumen et al. 2021
β-Ga_2O_3	The Chemical Vapor Deposition (CVD) method	Au catalysts	[26] Miao et al. 2021
Si	CVD reactor	employing Sn nanospheres as catalyst	[27] Mazzetta et al. 2021

InAs/InP	Molecular Beam Epitaxy (MBE)	gold catalyst	[28] Helmi et al, 2020[44] Ren et al. 2014
Poly (3-hexylthiophene) (P3HT) nanowires	N/A	N/A	[29] Jeong et al. 2020
Si-doped GaAs nanowires (NWs)	VS selective area growth patterned with SiO2 MBE	No catalysts	[30] Ruhstorfer et al. 2020
Ge	VLS-CVD	Au	[31] Li et al. 2011
II-VI semiconductors CdTe, CdS, ZnSe and ZnS	Vapor Liquid Solid (VLS) process	bismuth and tin	[32] Yang et al. 2010
GaAs, InAs and InGaAs nanowires	Molecular Beam Epitaxy (MBE)	gold as the growth catalyst	[33] Jabeen et al. 2009
Si	VLS-CVD	Al	[14] Wacaser et al. 2009
Si NWs On Si (100) and Si (111)	VLS-CVD	Gold catalyst	[34] Lindner et al. 2008

The included representative studies of some pioneer experimental work in the very recent years (2021 and 2020), with inclusion of some work of the previous decade, would present a general view of work on semiconductor nanowires. Among semiconductor materials, this study focuses on Si-NWs which are epitaxially grown in the CVD reactor using VLS bottom-up approach.

Original work of growing Si-NWs: catalysts span from auto Al

The nanowires growth using VLS can be undertaken in a Chemical Vapor Deposition (CVD) reactor or can be at the Molecular Beam Epitaxy (MBE). The CVD growth mechanism involves the absorption of source material from the vapor phase into a liquid droplet of catalyst above the solid substrate as explained in the original work of Wagner and Ellis, in 1969 [14]. The pioneer proposed VLS mechanism of growing Si-NWs using Au as a catalyst is based on three critical parameters: the presence of the arriving Si vapor atoms to the metal droplet in a liquid state acting as a preferred position on the solid substrate. The detailed growth conditions at the CVD such as the pressure, flow rate, and temperature are placed accordingly. On the other hand, the motivation for using Molecular Beam Epitaxy (MBE) to grow nanowires is that, although MBE growth is both complicated and challenging, its high precision and flexibility can give good control over the growth of thin layers and abrupt junctions, which may be an advantage in future nanostructure devices [35-37].

The cutting-edge technology of growing semiconductors for advanced applications is MBE where the control can be down to atomic level. MBE is an ultra-high vacuum technique that is used when thin films of the highest quality and perfection are required. Where Shuji Nakamura, University of California, Santa Barbara, awarded the Nobel Prize in 2014 on the invention of the blue InGaN LED [35]. Very recent work by Sadeghi et al. [36]. On growing $BaZrS_3$ chalcogenide perovskite thin films by MBE. The primary obstacle to success is the lattice and thermal expansion mismatches between the semiconductor compounds of interest and the silicon substrates. Novel heteroepitaxial growth technique, quasi van der Waals epitaxy, promises the ability to grow high quality As-based semiconductor compounds on silicon using a two- dimensional (2D) layered material as a buffer layer, where the van der Waals force is dominant between the layers, thus reducing the strain arising from lattice and thermal expansion coefficient mismatches.

The Nanoscale Chemical Templating (NCT) technique, which was invented in 2013 by Khayyat et al. controlling the position of growing Si-NWs using chemically active catalysts [37]. According to the binary phase diagram of Si and Au, as shown in Figure 3, the lowest melting temperature for the Au–Si eutectic is approximately 363°C obtained for a composition of Si and Au. The eutectic is lower than the melting point of Au (1064°C) and Si (1414°C) [21]. Considering that the liquid phase is thermodynamically equilibrated with the solid one, the lowering of the melting point, with the size of the droplet is given by equation 1, as follows [14].

Equation 1

$$\delta T = 2\sigma . T_0 / (\rho . L . r)$$

Where δT is the lowering of the melting point, σ is the interfacial energy,

T_0 is the melting point of the bulk metal, ρ is the material density,

L is the latent heat; r is the radius of the circle of the catalyst.

Thus, heating Au film deposited on Si substrate to a temperature of 363°C results in the formation of liquid Au–Si eutectic. The eutectic is simply a mixture of two elements at such proportions that its melting point is at the lowest possible temperature, much lower than the melting point of either of the two elements that make it up. If these Au–Si alloy droplets are placed in an ambient containing a gaseous silicon precursor such as silane (SiH_4), the precursor molecules decompose into Si and H_2 at the outer surface of the metal droplets, thereby supplying additional Si to the Au–Si alloy (Figure 3).

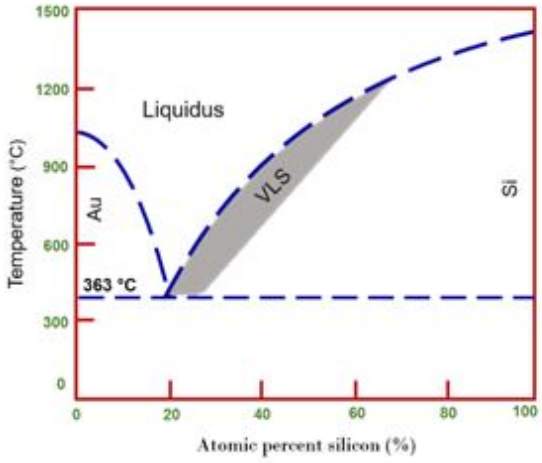

Figure 3: Phase diagram for the Au–Si system. The shaded zone represents the range of temperatures and alloy compositions at which VLS growth might occur [1].

It has been shown that Si-NWs grow perpendicularly on Si (111), as it is represented in Figure 4. However, the growth direction of the wires having same cross-section can be changed from <111> to <100> by any possible variation on one or more growth parameters including the growth temperature and the incoming reactant vapor concentration at the same, which can be attributed in term of surface/interface energy (Figure 4) [1,14-16].

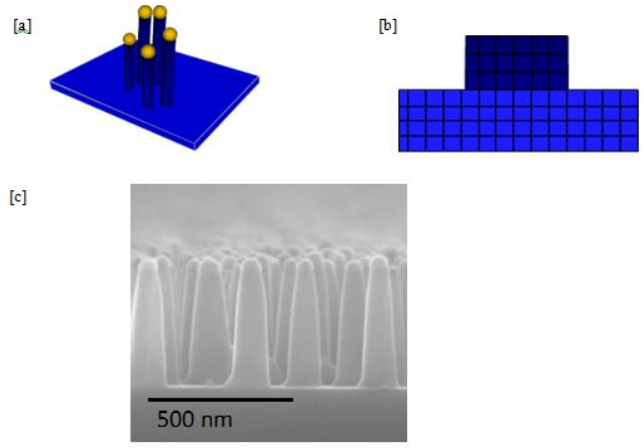

Figure 4: Schematic representation of epitaxial growth of Si-NWs (a), where the grown nanowires copy the crystal structure of the substrate, (c) epitaxial grown Si-NWs on Si (111) substrate

catalysed with Al, detailed growth conditions can be found at Khayyat et al. 2013 [38].

There are several derivatives of CVD systems exist; these can be classified by several parameters mainly the base and operation pressure, such as Ultra High Vacuum Chemical Vapor Deposition (UHVCVD). Since Si is known to oxidize easily, it is crucial to reduce the oxygen background pressure in order to be able to epitaxially grow uniform silicon nanowires. In particular, when oxygen-sensitive catalyst materials are used, it turns out to be useful to combine catalyst deposition and NWs growth in one system without breaking the vacuum in between [24,25].

It is often noted in VLS wire growth the radius of the catalyst droplet relates to the radius of the nanowire as described in Equation 2 [15].

Equation 2

$$R = r\sqrt{1/(1-(\sigma_{ls}/\sigma_l)^2)}$$

Where R is radius of the catalyst droplet, r is the radius of the nanowire, σ_l is the surface tension of the liquid catalyst, and σ_{ls} is the surface tension of the liquid catalyst interface. Based on this one can estimate the growth conditions and deduce the diameters of the catalyst droplet of the resulted growth of NWs with certain an average diameter. Manipulating the various related growth parameters of pressure, temperature and position are of critical importance for implementation of NWs as building units at various applications. The growth temperature has the greatest influence on the properties of Si-NWs. It not only changes the morphology but also affects the active doping of the as-grown wires. The strong influence of growth temperature on morphology is related to the selectivity of wire growth versus growth on the other surfaces; namely, the nanowire side walls and the (111) surface between the wires. This means that the surface facets of the side walls, the degree of tapering, and the growth rate on the Si (111) surface all depend on temperature.

Innovative approach of growing Si-NWs: nanoscale chemical templating technique

Controlling the growth position of a NW is important for fabricating devices, especially when involving a large array of nanowires. The growth reproducibility is critically a key parameter in the progress of implementing nanowires in advance applications. Free standing nanowires can be yielded and their position on the wafer can be determined by predefining the position of the seed on the wafer using lithography. There are several research groups working on optimizing the growth of positional Si-NWs [38]. Most of the studies to-date has used Au due to the convenience of handling that arises from its resistance to oxidation.

Nanoscale Chemical Templating (NCT) technique is a new method of controlling the spatial placement of the growth of Si-NWs catalyzed with oxygen reactive materials such as Al, which is a standard metal in silicon process line. The technique is

based about patterning a semiconductor substrate or other like substrate which is capable of forming Si alloy with Al during a following annealing step [25]. It is an innovate technique arises as a solution of the issue of the defective planar growth between the grown Si-NWs seeded with Al (or any other chemically active elements). The technique is called Nanoscale Chemical Templating (NCT) of oxygen reactive elements. Now, what does make NCT an innovative solution?[25].

NCT technique is a method involves the following advantages:

Does not require Al removal for selective growth (Figure 5 (I)).

Does not require any lithography steps (Figure 5 (II)).

Multiple application space (Figure 5 (III)).

As explained in Figure 5 (I) explains the process that does not require Al removal. (I-a) shows the patterned SiO_2 layer after photolithography, etching, and resist removal. (I-b) After Al deposition and annealing, notice the agglomerated Al:Si feature in the openings forming the NW seeds, while the Al in contact with SiO_2 has reacted with and roughened the surface. (I-c) After NW growth. The NWs are epitaxial and appear as bright spots in the plan view. In the cross-sectional view tapering is visible, due to a thin, non-seeded, Si layer thinner than 1/100 of the length of the nanowire. Notice that a single NW per opening is achieved. (I-c3), (I-c4) show a larger area containing both a patterned area on the right and an area with no oxide on the left where random growth occurs. The position control of Si-NWs can be achieved using silica microsphere, as described in Figure 5 (II). The schematic representation of spinning silica microsphere, where no lithography is required, on Si substrate, followed by thin layer evaporation of Al and the subsequent annealing as shown in (a) where (b) shows the Si-NWs growth. Patterning III-V semiconductors selectively is considered as one of the possible multiple applications schemes (III) [25]. The concept can be extended to forming novel patterning in III-V semiconductors (Figure 5 (III)). For example, Al reaction with GaAs will lead to formation of GaAl As selectively in exposed GaAs regions, thereby allowing obtaining patterned GaAlAs and GaAs regions adjacent to each other. Such structures have applications for optoelectronic and FET-like devices.

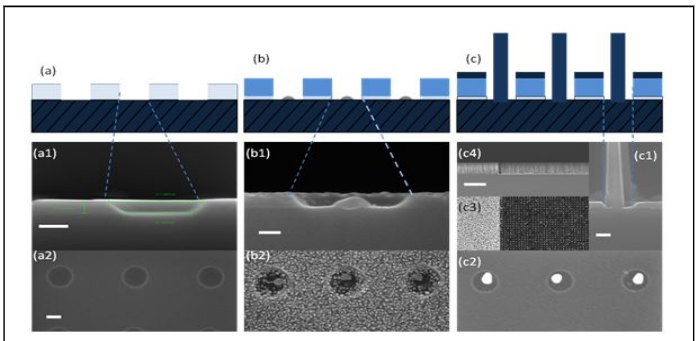

Figure 5 (I): (a)–(c) Schematic illustration of NCT of NWs with corresponding SEM images, cross-sectional ((a1), (b1), (c1) and (c4)) and plan view ((a2), (b2), (c2) and (c3)). The scale bars are: (a1) and (b1) 100 nm; (c1) 300 nm; (a2), (b2), and (c2) 1 μm; (c3) and (c4) 20 μm.

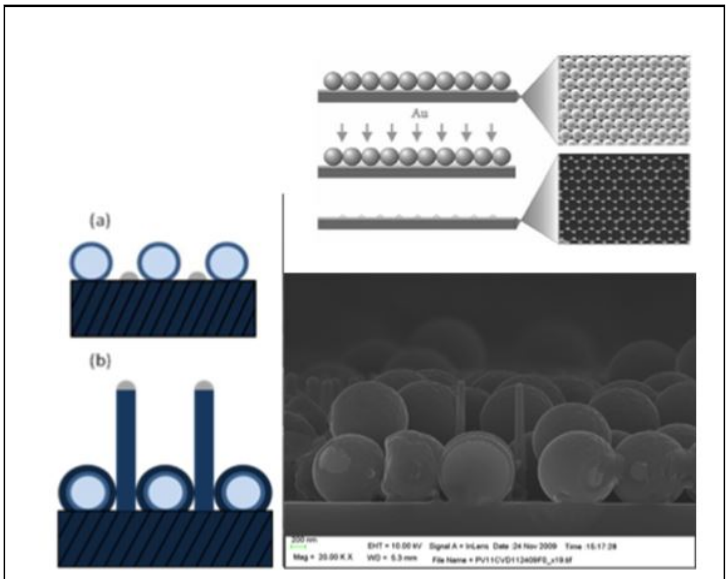

Figure 5 (II): Representation of NCT using silica microspheres (a and b), and the corresponding SEM original proof of the concept. II-a The microspheres dispersed on a Si substrate., after Al deposition and annealing, Al reacts with the oxide in the microspheres but on the substrate between the microspheres Al seeds form for NW growth. (II-b) On exposure to silane, NWs grow from seeds between the microspheres and unseeded growth occurs on the microsphere and substrate surface. A cross-sectional SEM image showing NWs growth between microspheres. Note the bright core of the microspheres, as shown by arrow 1 at both the schematic and SEM of the unoxidized silica (SiO2) and the darker contrast (marked as arrow 2) at the microsphere surface where the Al was deposited and the planner growth of Si was occurred.

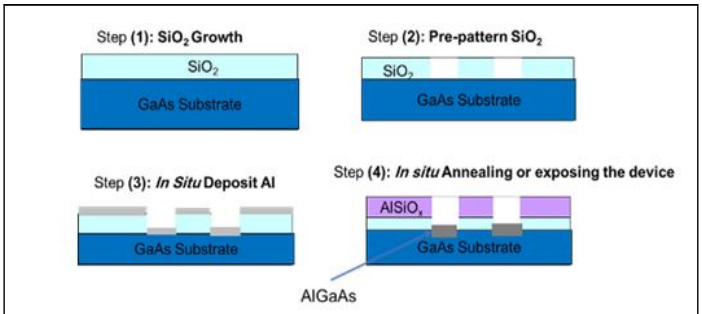

Figure 5 (III): Schematic representation of selective growth of AlGaAs for further applications.

To sum up, the spatial-controlled growth of nanowires is of potential interests for devices integration. It has been demonstrated experimentally a novel method of fabricating semiconductor nanowires on a surface of a semiconductor substrate in which the spatial placement of the semiconductor nanowires is controlled by using a patterned self-organized oxide layer and a non-oxidized oxygen reactive seed material.

APPLICATIONS ON NANOSCALE CHEMICAL TEMPLATING

Functional devices of Si-NWs

It is of great interest to find applications for Si-NWs, which could be as stands alone innovative structures such as in Photovoltaic (PV) cells or integrating with conventional structures such as Atomic Force Microscopy (AFM), and MOSFET, for the purpose of developing and miniaturizing (Figures 6-8) [26].

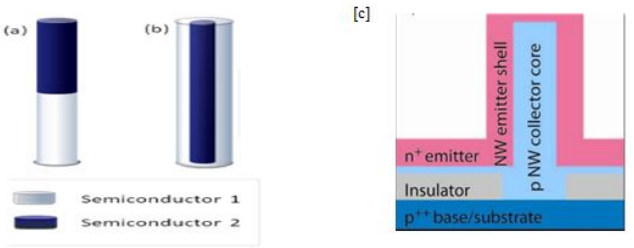

Figure 6: Schematic illustration of the main types of heterojunction nanowires. (a) Axial heterojunction. (b) Radial heterojunction (core-shell). (c) A core-shell PV cell [3].

Photovoltaic cells

PV Cells made of Si-NWs have several potential benefits over conventional bulk Si one or thin-film devices related primarily to cost reduction. It is possible to form the p-n core-shell junctions in high density arrays, which have the benefit of decoupling the absorption of light from charge transport by allowing lateral diffusion of minority carriers to the p-n junction which is at most 50–500 nm away rather than many microns away as in Si bulk solar cells. Based on this, the potential cost benefits come from lowering the purity standard and the amount of semiconductor material needed to obtain sophisticated efficiencies; increasing the defect tolerance; and lattice-matched substrates [6]. The concept of NWs-based PV cells has attracted the scientific community attention because of their potential benefits in carrier transport, charge separation and light absorption. The Lieber and Atwater and other groups have developed core-shell growth and contact strategy for their silicon p–n nanowire solar cells, with sophisticated efficiencies. Moreover, the ability to make single-crystalline nanowires on low-cost substrates such as Al foil and to relax strain in subsequent epitaxial layers removes two more major cost hurdles associated with high-efficiency planar solar cells. Catalysing the growth of Si-NWS and p or n doping the grown nanowires at the same time will be of potential importance for advanced applications of nanowires. Catalysts can be selected based on phase binary phase diagrams [1]. Silicon doping means the introduction of impurities into the crystal to the defined modification of conductivity. Two of the most important materials silicon can be doped with, are boron (3 valences) and phosphorus (5 valence electrons). Other materials are aluminium, indium (3-valent) and arsenic, antimony (5-valent) [39].

A schematic representation is shown in Figure 6 where SiO_2 has been used as a separation layer between the planar defective growth, which occurs during NWs growth, and the substrate to enhance the performance of the PV core shell junctions [5,12]. The thickness of the depletion region is dependent on the doping densities. The width of this region can be small for high doping densities (e.g. ~50 nm for 1020 cm^{-3} in Si) or it can be large for low doping densities (3 μm for 1014 cm^{-3} in Si). For solar cells the ideal doping level lies somewhere in between these two extremes. The diameter of a typical 'nanowire' is 10-100 nm. This is smaller than the typical depletion region. Thus, it is important to be careful when designing the doping levels and thicknesses of the nanowires.

The main message of this sub section is that, we have examined the formation of silicon nanowires grown by self-assembly from aluminum collector particles. Under optimum growth conditions it is possible to produce excellent quality crystal nanowires with rapid growth rates, high surface densities, low diameter dispersion, and controlled tapering. Rectifying junctions of an array of silicon nanowires, catalysed by Al, were fabricated (Figure 7). The prepared junctions have exhibited slight light sensitivity, which yield relatively low energy conversion efficiency. However, the fact that silicon solar cells based on nanowires have very short p-n junctions which might increases the carrier collection in the core-shell of the nanowire structure. This advantage leads to a higher tolerance for material defects and allows the use of lower quality silicon (Figure 7).

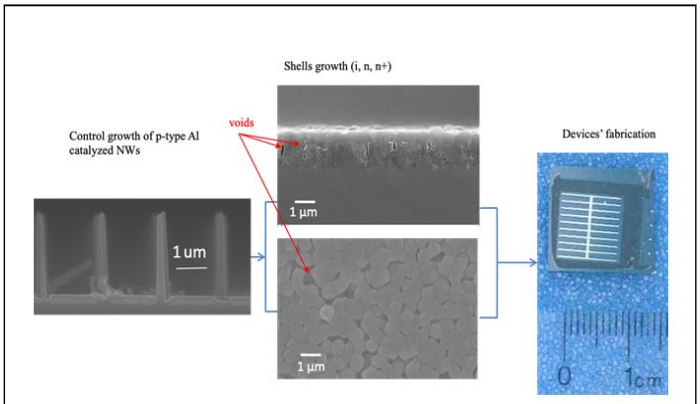

Figure 7: Growing Si-NWs (p-type) doped with Al using NCT, then forming shell of n-type building p-n junctions, where voids appear between formed junctions, finally fabricating the PV cells of 1 cm^2 surface area.

The above stated details of advantages and challenges of PV devices based on Si-NWs can be summarized as follows (Table 2).

Table 2: List of the main advances and challenges of PV cells based on Si-NWs technology.

Advantages	Short carrier diffusion length, good absorption of light.
	The shape and size of the Si-NWs based and 'voids' between junctions promote scattering.
	Low cost
	Si-NWs can be grown on cheaper substrates (we have grown Si-NWs on common Al foil).
	NWs have also been grown on reusable substrates.
Challenges	Depletion Region Width and Density.
	Forming an ideal p-n diode for core-shell Si-NWs by CVD is challenging, considering CVD switching precursors and forming defects at the interfaces.
	Surface Passivation.
	Reducing the amount of surface area, correlated with the risk of carrier recombination and loss at the surface that needs to be passivated is to fill in the void volume with emitter doped crystal.
	Isolation between Si-NWs.
	Reducing shunt resistances.

The possible advantages of integrating Si-NWs in relatively large scale solar cells make further investigations worth through simulation and experimental studies for future generation devices. The cumulative effort of various research groups, including ours have tried to outline and summarize some of the practical, technical, and inherent challenges which we have faced in producing large area (>mm^2) solar cells from core-shell Si-NWs and other related structures [40,41].

Atomic force microscopy

AFM is invented in 1968 where it has opened new perspectives for various micro and nanoscale surface imaging in science and industry. Nanotechnology has benefited from the invention of the AFM, and in turn AFM is developing based on the progress of Si-NWs growth techniques. Based on the NCT technique where the growth of Si-NWs is catalyzed using oxygen reactive materials such as Al, it has been proposed to improve the resolution of AFM tips in a production scale [26]. The concept of "Production Scale Fabrication Method for High Resolution AFM Tips" is demonstrated in Figure 8, along with the various steps of the Si-NW growth on the tip of the available Si (100) or Si (111) AFM tips. The grown Si-NW on the squared-base Si (100) tip is 45° tilted, while Si-NW grow perpendicularly on the tip of the AFM tip of the triangular base of Si (111) [32-35]. Where further reduction of the average wire diameter to the nanometer scale can be done *via* hydrogen annealing or oxidation [8,36-41]. As the diameter decreased, the hardness tended to increase from 4.4 to 11.3 GPa. Under bending, the Si-NWs demonstrated considerable plasticity (Figure 8) [42].

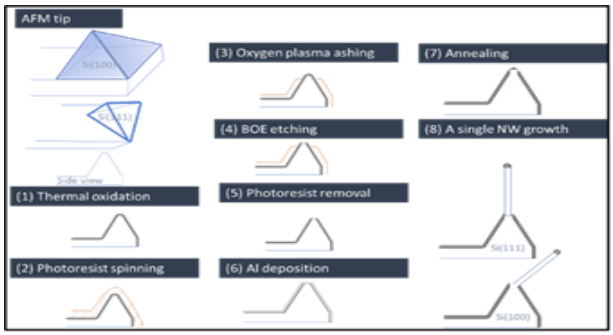

Figure 8: Schematic demonstration of detailed steps involved in Si-NWs integration with AFM tip, the square based Si (100) or the triangle based Si (111) cantilever were first oxidized forming SiO_2 (step 1), spinning photoresist (step 2), oxygen plasma etching the tip (step 3), BOE etching removing the oxide layer at the tip (step 4), photoresist removal (step 5), followed by Al deposition (step 6), annealing to ball-up the Al droplet at the tip (step 7), finally Si-NWs growth perpendicularly on Si (111) and tilted on Si (100) [26].

The proposed structure in Figure 8 has not yet experimentally demonstrated, the fabrication of the structure could be achieved by the described processes of NCT explained in Figure 5 (I), where it illustrates the potential mass scalability of this technique. A strategy has been presented to attach microcantilever beams with a single Si-NW scanning tips that

were directly grown by Au-catalyzed using VLS synthesis. The diameter or cross-section of Si-NWs produced by bottom-up methods such as VLS growth may be too large, including NCT technique, for some applications such as integration with AFM, in which case it is desirable to reduce the nanowire cross-section in a controlled manner. One of the possible techniques of reducing the diameters of Si-NWs is oxidation. The oxidation rate of silicon nanowires decreases with time or oxide thickness up to the point where oxidation is virtually stopped. This can be explained based on the compressive stress at the Si/SiO_2 interface which results in the self-limitation of the oxidation rate for long oxidation times, in good agreement with experimental data [8]. The self-limiting nature of nanowire oxidation can be used to tighten the diameter distribution of nanowires defined by lithography and plasma etching [43].

AFM measurements showed evidently that the assembled Si-NW scanning tips are suitable for topography reconstruction as well as overall comparable with conventional pyramidal scanning tips besides their high aspect-ratio nature and a superior mechanical durability [44-46]. Moreover, the growth direction can be tailored based on the required AFM investigations. On Si (111), NWs will grow perpendicularly, where as they grow 45° tilted on Si (100) surfaces.

Metal oxide semiconductor field effect transistors

MOSFET can be designed in the form of NWs, as shown in Figure 9 [8]. Employing Si-NWs as MOSFET channel can enable a gate-surrounding structure allowing an excellent electrostatic gate control over the channel for reducing the short-channel effects. The channel of the npn MOSFET can be altered using NWs as shown when a positive voltage is applied to the gate (p-type) the holes in the p-type semiconductor are repelled from the surface, and minority carrier conduction electrons are attracted to the surface. If the gate voltage exceeds the threshold value, then an inversion layer is created near the surface. In this layer the material behaves as an n-type and provides a conducting n-channel between the source and drain. The width of the conduction channel is dominated by the diameter of the NW. Where the presented a 3-D schematic diagram of the circular gate-all-around Silicon On Insulator (SOI) nanowire FET with z-axis physical symmetrical contraction, in a structure can be called resonant tunneling nanowire FET (RT-NWFET). The width of the tunnel barriers can be adjusted by the Length of the Contraction (LC) in the transport direction, i.e., the length of the integrated nanowire. On the other hand, the height of the tunnel barriers can be adjusted by varying the diameter of the grown nanowires, which is shown as the contracted cross-section. The obtained results showed the OFF-state current has been reduced while ON-state current has been compared to the conventional NWFET. Moreover, there are more key parameters have showed superior properties, where it can be speculated that, the built device *via* simulation, of RT-NWFET would be a promising candidate for the complementary MOSFET technology.

Moreover, effective integration of Si-NWs and MOSFET will result in modern Complementary Metal Oxide Semiconductor (CMOS) technology along with memory applications. The scaling of MOSFET continues with the emergence of new technologies to CMOS down to ever smaller technology node. Thus, compared to planar devices based on bulk materials, the Si-NWs have a smaller channel and large surface-to-volume ratio. In addition, the gate-surrounding or gate-all-around structure that can be formed in the Si-NWs MOSFET allows excellent electrostatic gate control over the Si-NWs channel. Moreover, the Si-NWs MOSFETs enable ultimate CMOS device scaling with the best possible short-channel control (Figure 9).

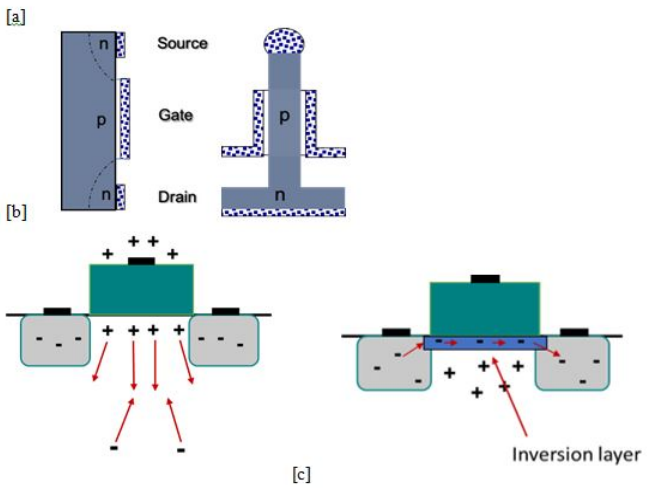

Figure 9: (a) shows a schematic representation of an (npn) MOSFET the conventional one, in parallel with the innovative one of NWs (b) shows the migrating of charges based on the applied voltages, and (c) presents the formation of the inversion layer, the channel across the diameter of the NW.

Because of the enhanced surface to volume ratio of NWs, their transport behavior may be modified by changing their surface conditions, and this property may be utilized for sensor applications to provide improved sensitivity compared to conventional sensors based on bulk material. Si-NWs sensors will potentially be smaller, more sensitive, demand less power, and react faster than their macroscopic counterparts [42-44].

Future remarks of nanowires research

In this review, we attempted to summarize progresses made in this field during the last several years, ranging from nanowire growth with precise control at the atomic level [41]. Probing novel properties in 1D systems using stands alone innovative novel device were presented, in addition to integration and assembly methods of large numbers of NWs for practical applications.

We conclude this review chapter with some outlooks for future research. Will nanowires research lead to new science or discovery of new phenomena? Will it lead to new applications? [47-50]. the answer is clearly yes based on the fact that research activity on the topic of nanowires. Studies of nanowire research are among the most potential in the topic of nanoscience, as shown in Figure 10. The cumulative published studies starting from 2010 up to 2020 on the topic of nanowires has been

increased markedly reflecting the technological importance of this topic (Figure 10).

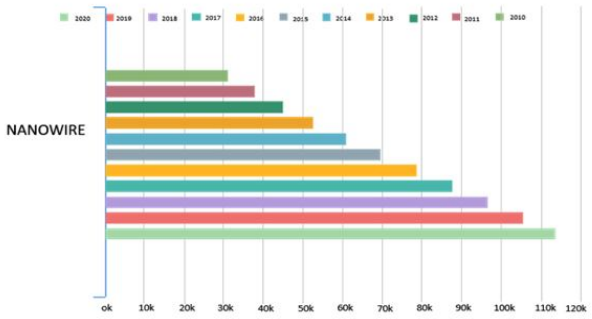

Figure 10: Cumulative nanowires publications in 11 years (2010-2020) (there is no data available for the 2021, where x-axis represents the number of articles in kilo, in 2020 there were more than 100,000 articles at the topic on nanowires, according to number of nanotechnology-related articles indexed in Web of Science (WoS) (ISI Web of Knowledge).

The ever-growing demand for smaller electronic devices is prompting the scientific community to produce circuits whose components satisfies size and weight requirements. The well-controlled NW growth process, with distinct chemical composition, structure, size and morphology, implies that semiconductor nanowires can be integrated within the process of the development of nanodevices. Control of the synthesis and the surface properties of Si-NWs may open new opportunities in the field of silicon nanoelectronics and use them as nanocomponents to build nano-circuits and nano-biosensors. Moreover, Si-NWs possess the combined attributes of cost effectiveness and mature manufacturing infrastructures [45-46].

The conventional thin film technologies using MBE growth method have run into interfacial lattice mismatch issues that often result in highly defective optical materials. In this regard, Si-NWs growth provides a possible mechanism for relaxing the lattice strain at the interface and provides dislocation-free semiconductor growth on lattice mismatched substrates, where, radial strain relaxation allows for uncharted combinations of semiconductor materials (III-V on Si). In this regard, efforts must be made to break new grounds in this promising research field to stimulate more creative ideas about nanowire research and applications. Many promising applications are now at the early demonstration stage, but are moving ahead rapidly because of their promise for new functionality, not previously available, to the fields of electronics, optoelectronics, biotechnology, magnetics, and energy conversion and generation, among others [47-49].

Integration of nanosystems and biosystems is a multidisciplinary research field that has the potential for tremendous impact on various applications the combination of these widely diverse areas of research promises to yield revolutionary advances in healthcare, medicine, and the life sciences. Moreover, it might end up with creation of new and powerful tools that enable direct, sensitive, and rapid analysis of biological and chemical species [50-51]. To simulate future research on NWs, one would look at the progress achieved by the industries of semiconductors which have produced devices and systems that are part of our daily lives, including sensors, lasers, light-emitting diodes, solar panels, computers and cell-phones [52-54]. Then, imagine changing the semiconductors morphology from bulk to nanowire form, one might wonder how much fundamental difference there is and size reduction of our current electronics tools. Where, sometimes the intersection of top-down and bottom-up approaches toward building nanostructures for practical functionality is also possible.

CONCLUSION

To sum up, semiconductors will continue to inspire us and improving our life quality *via* continuous dedicative research activities, overcoming the current fabrication barriers [55-58]. MOSFET is the key unit of electronic industries, microprocessors, memory chip, and telecommunications circuits. Based on this, any possible limitations with MOSFET technologies, will consequently affect the other related applications [55-58]. Moore observed an exponential doubling in the number of transistors in every 18 months through the size reduction of transistor components. This limitation is directly related to the fact that we cannot break down the atomic size barrier, which implies a fundamental size limit at the atomic/nucleus scale. After all, there is no more direct 18-month doubling, instead there are other forms of transistor doubling may happen at a different slope, which opens doors for more research on nanowires and other nanotechnological unit integration [8]. Simulation models of suggested device structures can provide foresight report of the possible approaches of the various available nanostructure integrations [59-60].

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