OPEN ACCESS Freely available online

Journal of Remote Sensing & GIS

Review Article

Minimizing the Delay of C2MOS D Flip Flop using Logical Effort Theory

Swarnima Trivedi*

Department of Engineering and Technology, Mody University of Science and Technology, Lakshmangarh, India

ABSTRACT

Future Electronics has a full selection of Binary counters or Frequency dividers such as Radio Frequency divider, digital frequency divider, analog frequency divider which can further be used for improving the performance of electronic counter measures equipment's, communications systems and laboratory instruments. An arrangement of D Flip Flops is a classical method of designing a Frequency Divider. There is vast variation encountered in digital circuits because of scaling and process imperfections. So this paper deals with D flip-flop circuit in terms of propagation delay. The task is to minimize the propagation delay of D flip-flop blocks using Logical Effort Theory which is further used in designing binary counter.

Keywords: Frequency Divider; Counter; C2MOS; Logical Effort Theory

INTRODUCTION

Sequential logic is a type of logic circuit where output not only depends on the present value of its input signals but also on the sequence of past inputs unlike combinational logic, where output is a function of only the present inputs.

The basic memory element in sequential logic is the bistable latch or flip-flop. Sequential circuits can be synchronous or asynchronous depending upon the construction of clock signal i.e. in synchronous circuits the internal state of the circuit change their state simultaneously with the given input clock signal whereas in asynchronous circuits clock signal ripple through stages to achieve the next state.

This paper is organized as follows: Section 2 describes D flip flop symbol , clocked inverter circuit; Section 3 describes the logical effort technique for delay minimization; Section 4 describes the design specification for D Flip Flop designed by C2MOS technique using Logical Effort Theory; Section 5 presents the simulation results and the conclusion is given in Section 6.

THE CLOCKED INVERTER

D Flip-flops are used as a part of memory storage elements and data processors also they are simpler in terms of wiring connection as compared to JK flip-flop. The major applications of D flip-flops are to introduce delay in timing circuit, as a buffer, sampling data at specific intervals etc. The symbol of D Flip Flop is shown in Figure 2.1. The clock signal has to be high for the inputs to get activated and whenever the clock signal is LOW, the output remains unaffected. C2MOS design uses clocked inverter shown in Figure2.2. The circuit combines the static logic with synchronization which is achieved through clock signals. It is just like an ordinary inverter except that it is controlled by a set-signal i.e. c' and c [1]. These are normally connected to the clock signal so that the inverter either inverts while the clock is low or while it is high.

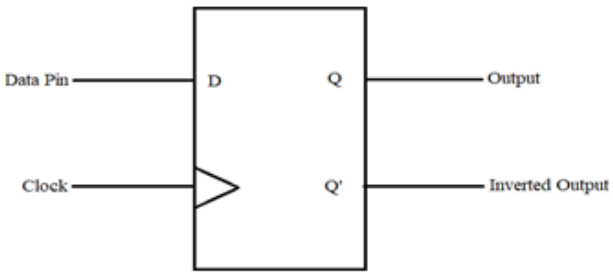

Figure.2.1.The D flip flop symbol

Many efforts have been done to enhance the performance of D flip flop. The method of logical effort is the easiest way to estimate delay in a CMOS circuit.

***Correspondence to:** Swarnima Trivedi, Department of Engineering and Technology, Mody University of Science and Technology, Lakshmangarh, India; Tel No: 9166305026; E-Mail: swarnimatrivedi1996@gmail.com

Received date: May 26, 2021; **Accepted date:** September 14, 2021; **Published date:** September 24, 2021

Citation: Trivedi S (2021) Minimizing the delay of C2MOS D flip flop using Logical effort theory. J Remote Sens GIS 10: p747

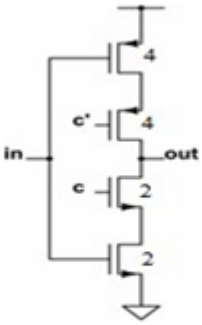

Figure.2.2.The Clocked inverter

In particular Transistor Sizing is effective method in reducing delay in particular circuit and through method of logical effort the proper number of logic stages on a path and the best transistor sizes for the logic gates can be estimated.

The scheme C2MOS D flip flop is presented in this paper to achieve better transition delay as compared with conventional design.

DELAY IN A LOGIC GATE

The logical effort of a logic gate is defined as the number of times worse it is at delivering output current than would be an inverter with identical input capacitance. In the method, the delay of a gate is estimated by modeling it as a linear function of the load being driven as:

D = g× cout/cin + p = g×h+ p

= f+p

Logical Effort (g) is the complexity of the gate, relative to a standard inverter circuit .i.e.

g =Cb/Cinv

=(Σb Ci)/Cinv

Where, Cb is the combined input capacitance of every signal. Electrical Effort, or Gain (h=cout/cin) describes how the electrical environment of the logic gate affects circuit performance and how the size of the transistors in the gate determines its load-driving capability in any circuit and Parasitic Delay (p) which is a fixed quantity expresses the intrinsic delay of the gate due to its own internal capacitance.

Acc. to Sutherland the minimum delay of any circuit is obtained by distributing the path effort F equally to each gate on the path. Parasitic delay (pinv) of inverter is normalized to unity for our purpose and

N-input NAND = n*pinv

N-input NOR = n*pinv

N-way mux = 2n*pinv

XOR = 4* pinv

Delay is the smallest when each stage bears some effort

⍰= F1/N

More importantly, it leads to a natural extension for estimating the minimum delay, D, of a path of complex logic as

D = NF1/N+P

Gate sizes required for calculating least delay

Cin = giCouti/⍰

While calculating logical effort length of transistor is kept constant and we capture transistor size by its width,w.As the capacitance of the transistor's gate is proportional to w and its ability to produce output current, or conductance, is also proportional to w [2]. We compute the logical effort as a ratio of capacitances, the units we use to measure capacitance may be arbitrary (as the quantity is ratioless). This observation simplifies the calculations largely. In CMOS processes, pullup transistors must be wider than pulldown transistors to have the same conductance or same resistance μ is defined which is μ = μn/μp is the ratio of PMOS to NMOS width in an inverter [3]. For simplicity, we will often assume that γ = μ = 2 which means an inverter will have a pulldown transistor of width w and a pullup transistor of width 2w, represents in Figure 3.1a, so the total input capacitance can be said to be 3w (i.e. 2+1=3).

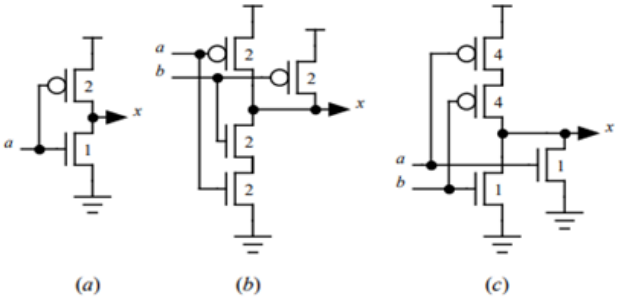

Figure.3.1 a) Inverter b) 2-input NAND Gate c) 2-input NOR Gate

Similarly we find the logical effort of the 2-input NAND, 2-input NOR gate in Figure 3.1b & Figure 3.1c respectively and of clocked inverter in Figure 2.2 by extracting capacitances from the circuit. The input capacitance of one input signal is equals to the sum of the width of the pulldown transistor and the pullup transistor [4], or 2+2 = 4 in NAND gate logic and similarly for 2- input NOR gate 4+1 = 5 shown in Figure 3.1c. The input capacitance of logic gates are compared with the input capacitance of the inverter with identical output drive is Cinv = 1+2 = 3. According to Equation, the logical effort per input of the 2-input NAND gate is therefore g = 4/3 and g = 5/3 for NOR gate.

Logical effort for clocked inverter is as below: For input in, gin = (4+2/3) = 2 Similarly for clock signal c,

gc = (4+2/3) = 2

gtotal = (2+2) =4

DESIGN SPECIFICATION FOR C2MOS COUNTER

The baseline counter circuit is shown in Figure 4.2 designed using C2MOS D flip flop because of its fast and low power

applications [5][6]. It is an inverter- based master-slave D flip-flop uses clocked inverters described in section 2 to control the loading value and breaking the feedback loop. The schematic for C2MOS D flip flop [7] is shown in Figure 4.1.

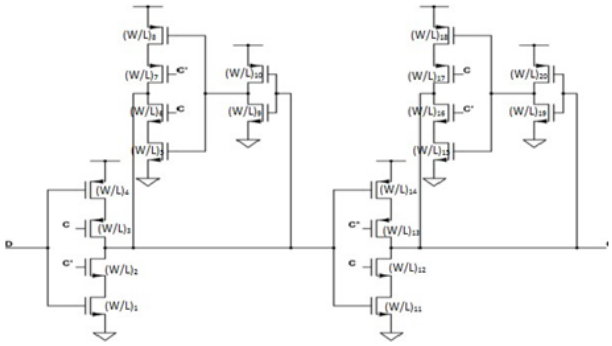

Figure.4.1 C2MOS D flip flop structure

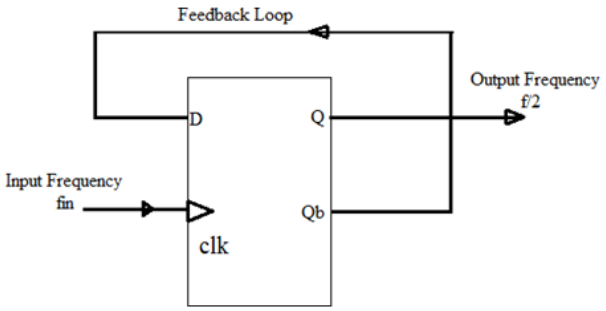

Figure.4.2 .Binary Counter

These are the following specifications keeping the parameters of first stage constant we calculated rest of parameters using logical effort theory for designing the flip flop of channel length L=0.18µm having 65fF load.

SIMULATION RESULTS

The logical effort model has been studied and tested using 180 nm CMOS technology on Mentor tanner tool

16.30 with 65fF load. The model is compared against the original one.

Table1: Transistor aspect ratio

Parameters	Values(µm)
(W/L)1=(W/L)2	1.2
(W/L)3=(W/L)4=2(W/L)1	2.4
(W/L)5=(W/L)6	1.03
(W/L)7=(W/L)8=2(W/L)5	2.07
(W/L)10=2(W/L)9	0.89
(W/L)11=(W/L)12	3.06
(W/L)13=(W/L)14=2(W/L)11	6.12
(W/L)15=(W/L)16	2.63
(W/L)17=(W/L)18=2(W/L)15	5.27
(W/L)20=2(W/L)19	2.26

Table 2: Delay comparison in DFF with or without LET

Delay	DFF without LET(in nsec)	DFF with LET(in nsec)
Delay Time	49.2190	48.5893
Average Delay	49.1136	48.3917

Table 3: Delay comparison in Counter circuit with or without LET

Delay	Counter without LET(in nsec)	Counter with LET (in nsec)
Delay Time	29.2188	28.5911
Average Delay	27.1149	26.3923

CONCLUSION

Use of Logical Effort methods for performance comparison of counter circuit is presented. Obtained results are found consistent with simulation and are encouraging that counter designed with LET technique is faster as compared to conventional design.

REFERENCES

1. S.Thomas Niba, "Analysis of shift register using integrated power and clock distribution networkbased master slave flip flop," Journal of theoretical and applied information technology,October 20,2015.
2. Sutherland, B. Sproull, D. Harris, "Logical Effort: Designing Fast CMOS Circuits," Morgan Kaufmann Publisher, 1999.
3. Kunwar Singh, Aman Jain "Optimum transistor sizing of CMOS logic circuits using logical effort theory and evolutionary algorithms," Integration, the VLSI Journal, August 7, 2017.
4. Satyajit Anand, Pradeep Kumar Ghosh," Optimization and Comparison of 4-stage inverter, 2-i/p 4-stage NAND gate, and 2-i/p 4 stage NOR gate Driving Standard Load by Using Logical Effort Theory ", AIP Conference Proceedings.
5. S.barra,N.Bouguechal, " Design and layout of finite state machine using C2MOS latch in CMOS 0.35µm technology" 2nd International Conference of Electrical Systems Design & Technologies, hammamet Tunisia, Nov 8-10,2008.
6. "Trade-offs between Performance and Robustness for Ultra Low Power/Low Energy Subthreshold flip flops in 65nm CMOS", Magne Vaernes, Published 2013.
7. Peng panfeng, "A Novel Flip-Flop circuit for Sub- threshold Application," 2017 International Conference on Circuits, Devices and System.