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A Comparative Study on Electrical Characteristics of Au/N-Si Schottky Diodes, with and Without Bi-Doped PVA Interfacial Layer in Dark and Under Illumination at Room Temperature

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Abstract

In order to see the effect of Bi-doped PVA interfacial layer on electrical characteristics, both Au/n-Si (MS) and Au/Bi-doped PVA/n-Si (MPS) type Schottky barrier diodes (SBDs) were fabricated, and their main electrical parameters were investigated using current-voltage (I-V) and capacitance-voltage (C-V) measurements, in dark and under illumination at room temperature. Forward bias semi-logarithmic I-V plots of these SBDs show two distinct linear regions, with different slopes in the low and intermediate voltage region. Such behavior in I-V plots was explained by two parallel diodes model. Experimental results show that the ideality factor (n), barrier height (ϕ_b), series and shunt resistances (R_s and R_{sh}), and the density of interface states/traps (N_{ss}) are strong functions of illumination level and applied bias voltage. The R_s values were determined from the I-V characteristics, by using both Ohm's law. The energy distribution profile of N_{ss} was also obtained from the forward bias I-V characteristics, by taking into account voltage dependent barrier height (ϕ_e) and ideality factor (n). It was found that Bi-doped PVA layer lead to a considerable decrease in the leakage current, R_s and N_{ss} and increase in R_{sh} and rectifier rate ($RR=I_F/I_R$). In conclusion, a thin Bi-doped PVA interfacial layer, considerably improved the diode performance, both in dark and under illumination.

Keywords: Au/Bi-doped PVA/n-Si (MPS); Schottky barrier diodes (SBDs); I-V and C-V measurements; Series resistance; Interface states

Introduction

In recent years, metal/metal doped polymer/semiconductor (MPS) structures, which are known as MPS type Schottky barrier diodes (SBDs), have gained great importance due to their potential applications in the microelectric industry, instead of classic metal/semiconductor (MS) and metal/insulator/semiconductor (MIS) type SBDs [1-12]. MS type SBDs, with a thin interfacial polymer layer, such as polyaniline, poly(alkylthiophene), polypyrrole, polythiophene, poly(3-hexylthiophene) and polyvinyl alcohol (PVA), have been investigated by chemists, physicists, and electrical engineers, as well due to potential applications and interesting properties of these polymers. Among these polymers, PVA nano-fabrics have attracted much attention due to its unique chemical and physical properties, as well as its industrial applications [13]. In general, PVA has a poor electrical conductivity, but this conductivity in PVA arises due to the high physical interactions between polymer chains, *via* hydrogen bonding between the hydroxyl groups and the doping metals, and is mainly dominated by the properties of the amorphous regions [13,14].

The performance and reliability of the MS, MIS and MPS type SBDs is considerably influenced by the interface quality and shape of barrier formation between metal and semiconductor, surface preparation, formation of an interfacial layer, and it's thickness and homogeneity, doping concentration of semiconductor, density distribution of interface states (N_{ss}) between interfacial layer and semiconductor, series resistance (R_s), and sample temperature and applied bias voltage [15-20]. Among them, especially N_{ss} and R_s of device are important for practical applications and understanding the electrical characteristics.

Therefore, in this study, the forward and reverse bias I-V and C-V characteristics of Au/Bi-doped polyvinyl alcohol (PVA)/n-Si type SBDs were investigated at room temperature, under dark and illumination. In addition, the energy density distribution profile of N_{ss} was obtained from the forward bias I-V characteristics, by taking into account voltage dependent barrier height ($\phi_B(V)$) and ideality factor n(V). Experimental results show that the Bi-doped interfacial PVA layer led to considerable decrease in the leakage current, R_s and N_{ss} and led to increase in R_{sh} and rectifier rate ($RR=I_F/I_R$). So, it can be said that Bi-doped PVA considerably improved the performance of SBD.

Experimental Procedure

For the fabrication of Au/PVA (Bi-doped)/n-Si (MPS), (phosphor doped) single crystal silicon with surface orientation, 350 μm thickness and 0.7 Ω.cm resistivity was used. Si wafer was degreased in organic solution of peroxide-ammoniac solution in 10 minutes, and then etched in a sequence of H_2O+HCl solution, and finally quenched in de-ionized water resistivity of 18 MΩ.cm for a prolonged time. Preceding each cleaning step, the wafer was rinsed thoroughly in de-ionized water. Immediately after surface cleaning, high purity (99.999%) gold (Au), with a thickness of ~2000Å, was thermally evaporated onto the whole back side of Si wafer, in a pressure about 10^{-6} Torr in high vacuum metal evaporation system. In order to perform a low resistivity ohmic back metal contact, n-Si wafer was sintered at about 450°C for 5 min in N_2 atmosphere.

Immediately after the formation of ohmic contact, 0.5 g of bismuth acetate was mixed with 50 g of polyvinyl Alcohol (PVA), molecular

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weight=72,000 and 9 ml of de-ionize water. After vigorous stirring for 2 h at 50°C, a viscous solution of PVA/(Bi doped) acetates was obtained. The solution of the PVA (Bi-doped) was homogenized for 1.5 h by mixing with rotation, before the deposition. The PVA (Bi-doped) nanofiber film on n-Si substrate was coated by electro spinning technique. Electro spinning process utilizes electrical force to produce polymer fibers. Electro spinning setup consists of four major components: The high-voltage power supply, the spinneret, the syringe pump and the electrically conductive collector. In this system, using a peristaltic syringe pump, the precursor solution was delivered to a metal needle syringe (10 ml), with an inner diameter of 0.9 mm, at a constant flow rate of 0.02 ml/h. The needle was connected to a high voltage power supply and positioned vertically on a clamp. A piece of flat aluminum foil was placed 15 cm below the tip of the needle to collect the nanofibers. Si wafer was placed on the aluminum foil. Upon applying a high voltage of 20 kV on the needle, a fluid jet was ejected from the tip. The solvent evaporated and a charged fiber was deposited onto the Si wafer, as a nonwoven mat. After spinning process, circular dots of 1 mm in diameter and 1000 Å thick high purity Au rectifying contacts were deposited on the PVA surface of the wafer, through a metal shadow mask in high vacuum system, in the pressure of about 10^{-7} Torr. In order to compare Au/PVA (Bi-doped)/n-Si (MPS) with Au/n-Si (MS), before spinning process, circular dots of 1 mm in diameter and 1000 Å thick Au was also deposited on the n-Si in same condition.

The forward and reverse bias *I-V* and admittance, which includes *C-V* and *G/ω-V*, measurements were performed by the use of a Keithley 2400 source meter and an HP 4192 A LF impedance analyzer and test signal of 40 mV_{rms} in dark and under illumination at room temperature, respectively. The measurement system is given in figure 1. 200 W solar simulator (Model: 69931 Newport-Oriel Instruments, Stratford, CT, USA) (Figure 1), was used as the light source. The photons at different power levels passed through an AM1.5 filter, which allowed wavelengths only between 400 and 700 nm to be incident upon the diodes.

Formation of Schottky/Rectifier contacts

After spinning process, circular dots of 1 mm in diameter and 1500 Å thick high purity Au rectifying contacts were deposited on the PVA surface of the wafer, through a metal shadow mask in liquid nitrogen trapped oil-free ultra-high vacuum system, in the pressure of about 10^{-7} Torr. All measurements were carried out with the help of a microcomputer, through an IEEE-488 AC/DC converter card in the Janis vpf-475 cryostat, to reduce the noise effect. Thus, the Au/n-Si Schottky barrier diodes (SBDs), with and without interfacial Bi-doped PVA layer, were fabricated in same conditions, and they will be named as MS and MPS type SBDs throughout the manuscript. Schematic cross-section of the Au/Bi-doped (PVA)/n-Si (MPS) is given in figure 2.

Results and Discussion

Forward and reverse bias I-V characteristics

The forward and reverse bias I-V characteristics of MS and MPS type SBDs in dark and under illumination conditions are given in figures 3a and b, respectively. As can be seen in these figures, the semi-logarithmic I-V characteristics of these diodes show a good rectifier behavior, especially in dark condition, i.e. while the reverse current shows weak voltage dependence, the forward current increases exponentially with the applied bias voltage. As can be seen in figure 3b, the forward bias semi-logarithmic I-V characteristics of these diodes show two distinct linear regions, with different slopes in the low and intermediate voltage regions. Such behavior of I-V was explained by two parallel diodes model. It is clear that the rectifier rate (RR) for the MPS type SBD is considerably higher (two order) than MS type SBD. On the other hand, as can be seen in figure 3b, the semi-logarithmic I-V plots under illumination condition show only one linear region in intermediate voltages. The reason of disappearance of the first linear region can be explained by open circuit voltage (V_{oc}). It is clear that under illumination condition, the value of V_{oc} is about 0.40 V for both SBDs; especially, the effect of white light on the MPS type SBD is such that the reverse current increases by almost three orders, when white light is dropped on the diode. Also, the magnitude of leakage current in the reverse bias region for MPS type SBD is 100 times lower than that of MS type SBD in dark condition. According to Demirezen et al. [1] Defives et al. [21] Ewing et al. [22], these two linear regions in the forward bias I-V plots in dark show two distinct barrier heights (BHs) in the parallel. Thus, the relationship between the I and V in dark can be expressed as [1,23-25].

$$I = I_{o1}\left[\exp\left(\frac{q(V - IR_s)}{n_1 kT}\right) - 1\right] + I_{o2}\left[\exp\left(\frac{q(V - IR_s)}{n_2 kT}\right) - 1\right] + \frac{(V - IR_s)}{R_{sh}} \quad (1)$$

Here, I_{o1} and I_{o2} are the reverse saturation currents, n_1 and n_2 are the diode ideality factors, which are corresponding to linear regions I (low bias region: LBR) and II (high bias region: HBR), respectively. R_s and R_{sh} are the series and shunt resistance of these diodes, respectively; the IR_s term is voltage drop on the R_s. In addition, the first and second terms in equation 1 may describe the diffusion and recombination generation current components, respectively. Thus, the equivalent circuit for two parallel diodes model can be illustrated in figure 4 [1]. In equation1, the terms of I_{o1} and I_{o2} can be extracted from the straight-lines intercept of

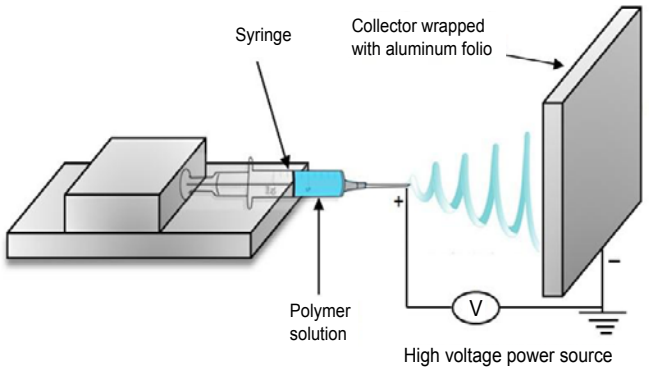

Figure 1: Schematic representation of the electrospinning process.

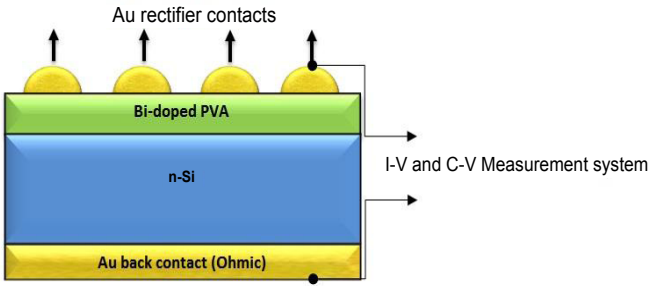

Figure 2: Schematic diagram of the Au/(Bi-doped-PVA)/n-Si SBD.

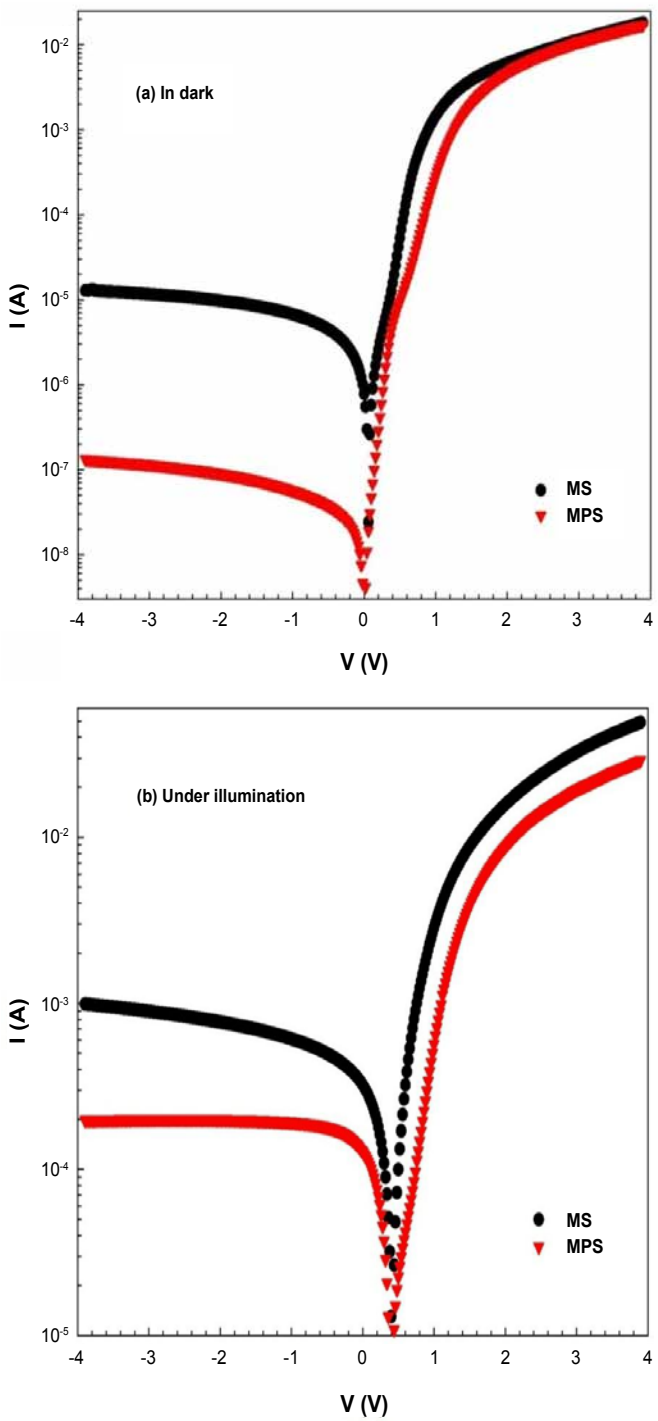

Figure 3: The forward and reverse bias I-V characteristics of MS and MPS type SBDs in dark and under illumination conditions.

lnI-V plots at zero bias, and can be expressed as:

$$I_{o1} = AA^{*}T^{2}\exp\left(-\frac{q\Phi_{Bo1}}{kT}\right) \quad I_{o2} = AA^{*}T^{2}\exp\left(-\frac{q\Phi_{Bo2}}{kT}\right) \qquad (2)$$

Where A is the rectifier contact area, A^{*} is the Richardson constant (120 $A.cm^{-2}$ K^{-2} for n-type Si), and $_{Bo}$ is the zero bias apparent barrier height, and equation 2 can be obtained by using the value of A and I_o as:

$$\Phi_{Bo1} = \frac{kT}{q}\ln\left(\frac{AA^{*}T^{2}}{I_{o1}}\right) \quad \Phi_{Bo2} = \frac{kT}{q}\ln\left(\frac{AA^{*}T^{2}}{I_{o2}}\right) \qquad (3)$$

The ideality factor is introduced to take the deviation of the experimental I-V data from the ideal thermionic emission (TE) theory into account. The n values of MS and MPS type SBDs were also calculated from the slope of the two linear regions of the forward bias I-V plots with different slopes as:

$$n_1 = \frac{q}{kT\tan\theta_1} \quad n_2 = \frac{q}{kT\tan\theta_2} \qquad (4)$$

The obtained experimental values of I_o, n and ϕ_{Bo} for the MS and MPS type SBDs in dark and under illumination conditions were given in table 1. As can be seen in table 1, the high values of n for two type SBDs show that the structures follow an MIS or MPS SBD configuration, rather than an MS SBD. Such behavior of n can be attributed to the existence of an interfacial layer, a wide distribution of low barrier height patches, a tunneling mechanism, and the particular distribution of N_{ss} at the M/S interface [15,16,20,26]. In addition, as can be seen in table 1, the diode ideality factor for the region II is much higher than the region I. This indicates that the value of n depends on applied bias voltage. On the other hand, these high values of n for two regions can be attributed to the high density of N_{ss} localized at M/S interface and the effect of barrier in homogeneity [1,8,11]. Also, the image-force effect, recombination-generation and tunneling may be possible mechanisms that could lead to an ideality factor value greater than unity [19-26]. On the other hand, unless specially fabricated, a SBD possesses a thin interfacial native layer at M/S interface. The existence of such an interfacial layer native or deposited can have strong effects on the main diode parameters.

The downward curvature in semi-logarithmic I-V plots at sufficiently high bias region in figure 3a and b were caused by the effect of R_s, rather than the N_{ss}. It is well known while the N_{ss} is significant in the low and intermediate bias regions; the R_s are effective only at high bias region. As can be seen in figure 4, the values of R_s and shunt resistance (R_{sh}) are both very important parameters of SBDs, because when a voltage is applied to a MS or MIS/MPS diodes, the applied bias voltage is shared by interfacial layer at M/S interface, depletion layer and R_s of the diode/structure. The magnitude of this shared applied voltage depends on the interfacial layer thickness, R_s and R_{sh} [1,15,16].

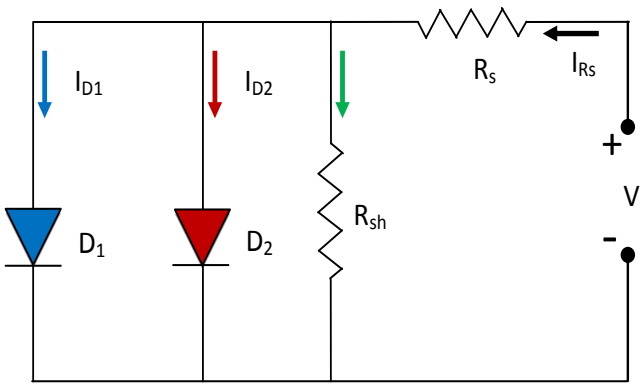

Figure 4: The equivalent circuit for two parallel diodes models. D_1 and D_2 are the first and second diode, respectively, R_s is the series resistance and R_{sh} is the shunt resistance.

Therefore, the performance and the reliability of these devices especially depend on this interfacial layer quality, its thickness, R_s and R_{sh}. The R_{sh} and R_s values were determined from the $R_i(=dV_i/dI_i)$ *vs* applied bias voltage (V_i) plots, which are given in figure 5. As can be seen in figure 5, that, at sufficiently high forward and reverse bias voltages, the R_i of MS and MPS reaches constant values, which are corresponding to R_s and R_{sh} values, respectively. The values of R_s and R_{sh} in dark were found as 220 Ω and 0.35 MΩ, and 250 Ω and 32 MΩ for MS and MPS SBDs, respectively. On the other hand, these values under illumination condition were found as 80 Ω and 0.48 kΩ, and 142 Ω and 20.05 kΩ for MS and MPS SBDs, respectively. It is clear that R_s and R_{sh} are both strong functions of voltage and interfacial layer.

The energy density distribution profile of the interface states (N_{ss}), which are in equilibrium with the semiconductor, can be determined from the forward bias I-V data, by taking into account the voltage dependent ideality factor n(V) and effective barrier height (ϕe). For the SBDs with an interfacial insulator or polymer layer, the ideality factor n becomes greater than unity, and the values of N_{ss} proposed by Card and Rhoderick [20] can be simplified and given as:

$$N_{ss}(V) = \frac{1}{q}\left[\frac{\varepsilon_i}{\delta}(n(V)-1) - \frac{\varepsilon_s}{W_D}\right] \quad (5)$$

where δ is the thickness of interfacial layer, W_D is the depletion layer width, ε_i and ε_s are permittivity of the interfacial layer and the semiconductor, respectively. Thus, in n-type semiconductors, the energy of N_{ss} (E_{ss}) with respect to the bottom of conduction band (E_c), at the surface of the semiconductor, can be obtained according to Rhoderick and Williams [16] and Card and Rhoderick [20]. The value of W_D is obtained from the experimental C^{-2}-V plots for each illumination level at 1 MHz. Furthermore, for *n*-type semiconductors, E_{ss} with respect to E_c at the semiconductor surface is given by

$$E_c - E_{SS} = q(\Phi_e - V) \quad (6)$$

Figure 6a and b show the energy density distribution profiles of N_{ss}, with and without interfacial Bi-doped PVA layer (MS and MPS) in dark and under illumination cases at room temperature, respectively. As can be seen in these figures, there is exponential increase in N_{SS} from the nearly mid-gap of semiconductor toward the bottom of the conductance band for MS and MPS type SBDs both. It is clear that the donor type N_{ss} is in effect near the conductance band. Also at any specific energy, the values of N_{ss} for MPS type SBD for two cases are less compared to MS type SBD. The purpose of the Bi-doped PVA layer is to prevent the reaction and inter diffusion between the metal (Au) contact and semiconductor (Si) surface, and reduce the high gate leakage current and N_{ss}. The decrease in the leakage current in the MPS type SBD is caused by the thin interfacial layer, and is due to a combination of increased barrier height at M/S semiconductor interface and reduced velocity of charge carriers.

IN DARK						
	REGION I			REGION II		
	I_o (A)	n	ϕ_{Bo} (eV)	I_o (A)	n	ϕ_{Bo} (eV)
MS	2.27×10^{-7}	3.303	0.732	2.58×10^{-7}	3.716	0.729
MPS	9.24×10^{-9}	2.314	0.815	4.56×10^{-7}	6.315	0.714
UNDER ILLUMINATION						
	REGION I			REGION II		
	I_o (A)	n	ϕ_{Bo} (eV)	I_o (A)	n	ϕ_{Bo} (eV)
MS	-	-	-	3.58×10^{-7}	3.572	0.720
MPS	-	-	-	8.53×10^{-7}	6.174	0.698

Table 1: The obtained I_o, n and ϕ_{Bo} values for the MS and MPS type SBDs in dark, and under illumination conditions.

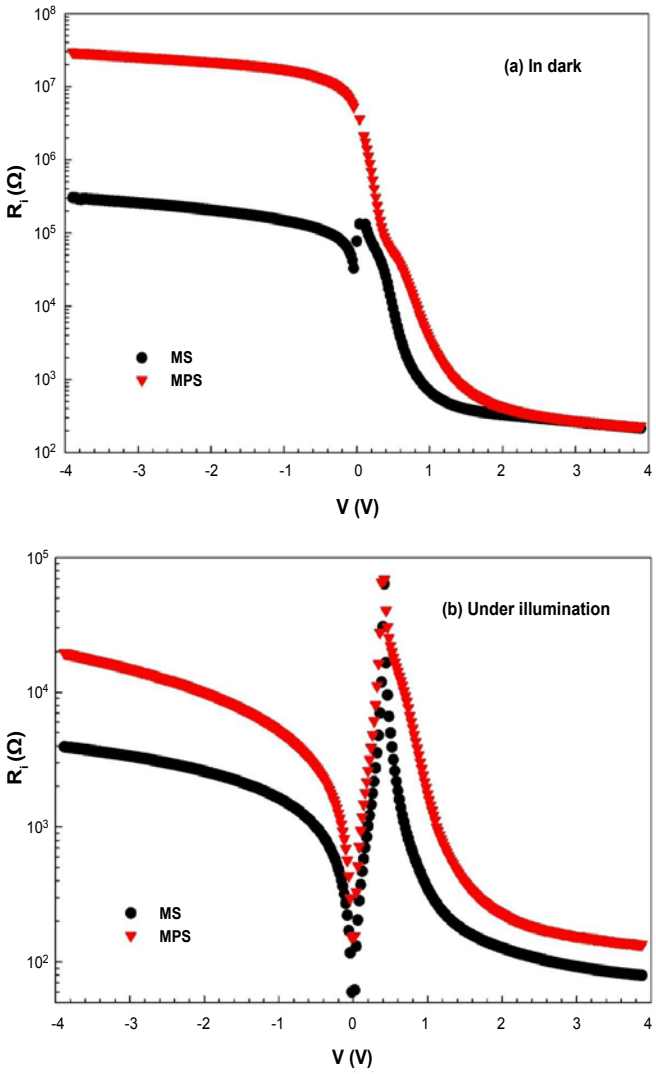

Figure 5: The plot of the structure resistance vs applied bias voltage for MS and MPS type SBDs **(a)** in dark and **(b)** under illumination conditions.

Effects of illumination on the C-V and G/ω-V characteristics

At sufficiently high frequencies ($f \geq 1$ MHz), the N_{ss} cannot follow the (ac) signal, because at high frequencies, the carrier life time (τ) is larger than the measured period [27]. Therefore, forward and reverse bias *C-V* and *G/ω-V* characteristics of MS and MPS type SBDs in the dark and under illumination at room temperature and 1 MHz were given in figures 7a and b, and 8a and b, respectively. As can be seen in figure 7, the C-V plots in dark and under illumination show three distinct regions, which are called as inversion, depletion and accumulation regions. The values of C increase with increasing applied bias voltage. However, the behavior of the C-V curves is different for each region for two samples. C and G/ω values of MS and MPS type SBDs increase under illumination effect. But, as can be seen in figure 8, especially the values of G/ω increase considerably under illumination. It is well known when photons' energy is greater than energy band gap of semiconductor (E_g), it may lead to generation of electron hole pairs

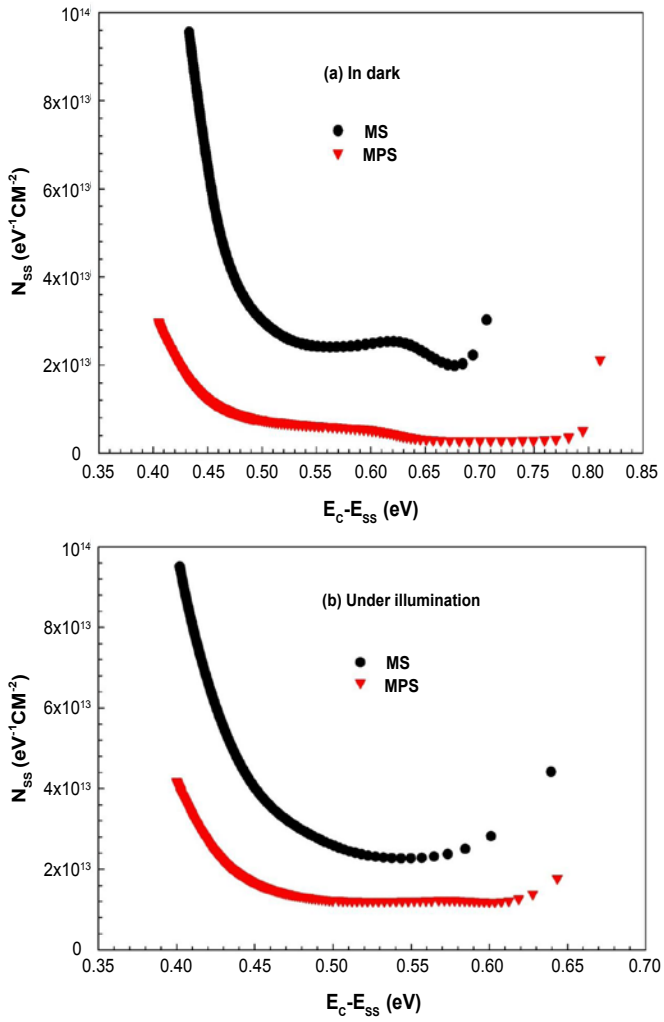

Figure 6: The energy distrubition profile of the N_{ss} obtained from the forward bias *I-V* characteristics of MS and MPS type SBDs **(a)** in dark and **(b)** under illumination conditions.

in the depletion region of the semiconductor. After that, the structures are stressed with an electric field, these electron-hole pairs would be separated by the strong local internal electric field at grain boundaries. Electrons are swept out of the insulator/polymer layer quickly by the electric field, while the holes are swept slowly and hence, could be trapped by the defects. Consequently, there would be an additional photo capacitance and conductance in the diodes.

It is clear that especially the behaviour of C-V and G/ω-V plots is different from region to region under illumination effect. Such behaviour of C-V and G/ω-V plots can be attributed to the restructure and reordering of charges at interface under illumination effect. The decrease in resistivity or the increase in conductivity may be the other reason of such behaviour of C and G/ω values, under illumination effect.

When C-V measurement are carried at sufficiently high frequencies ($f \geq 1$ MHz), the depletion layer capacitance in a MS and MIS/MPS SBDs can be expressed as [15,16].

$$C^{-2} = \frac{2(V_D + V)}{q\varepsilon_s N_D A^2} \quad (7)$$

Where A is the rectifier contact area of diode, V is the applied reverse bias, N_D is the donor concentration and V_D is diffusion potential at zero bias, and is determined from the extrapolation of the linear part of the C^{-2}-V plot (Figure 9) to the V axis. As can be seen in figure 9, C^{-2}-V plots are linear in the wide bias range in the inversion region. In MPS type SBDs, C^{-2}-V plot gives a peak both in dark and under illumination condition due to the effect of R_s and particular density distribution of N_{ss}. Thus, the value of barrier height $\varphi_B(C\text{-}V)$ can be obtained by the relation.

$$\Phi_B(C-V) = V_0 + \frac{kT}{q} + E_F - \Delta\Phi_B = V_D + E_F - \Delta\Phi_B \quad (8)$$

Where V_o is the intercept voltage, kT/q is thermal energy and E_F is the energy difference between the bulk Fermi level and conductance band edge, and it can be obtained from the following relation:

$$E_F = \frac{kT}{q}\ln\left(\frac{N_c}{N_D}\right) \quad (9a)$$

With

$$N_c = 4.82\times10^{15}T^{3/2}\left(\frac{m_e^*}{m_0}\right)^{3/2} \quad (9b)$$

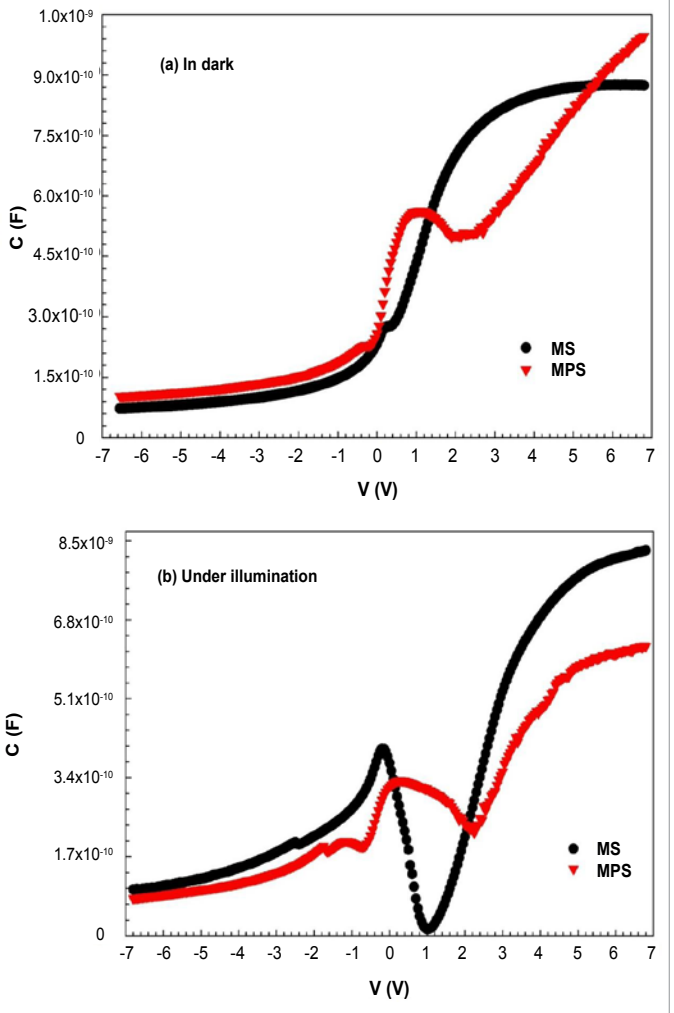

Figure 7: Measured capacitance *C* vs *V* of MS and MPS type SBDs **(a)** in dark and **(b)** under illumination conditions.

Where N_c is the effective density of states in Si conductance band, m_e^* is the effective mass of electrons [15,16] and m_o, the rest mass of the electron. In Equation (8), $\Delta\phi_B$ is the image force barrier height lowering, and is given by Sze [15].

$$\Delta\varphi_B = \left[\frac{qE_m}{4\pi\varepsilon_s\varepsilon_o}\right]^{1/2} \quad (10a)$$

Where E_m is the maximum electric field and given by

$$E_m = \left[\frac{2qN_DV_o}{\varepsilon_s\varepsilon_o}\right]^{1/2} \quad (10b)$$

After knowing the above values, the value of barrier height of ϕ_B(C-V) can be obtained from the reverse bias C^{-2}-V characteristics by using Equation 8. The obtained experimental values of V_o, N_D, E_F, W_D,E_m,$\Delta\phi_B$ and ϕ_B(C-V) values for MS and MPS type SBDs are given in table 2. As can be seen in tables 1 and 2, the value of ϕ_B(C-V) is higher than the value of ϕ_{Bo} obtained from forward bias I-V data, for both SBDs in dark and under illumination conditions.

The difference between barrier heights (BHs) obtained from I-V and C-V measurements is mainly due to the inhomogeneities.

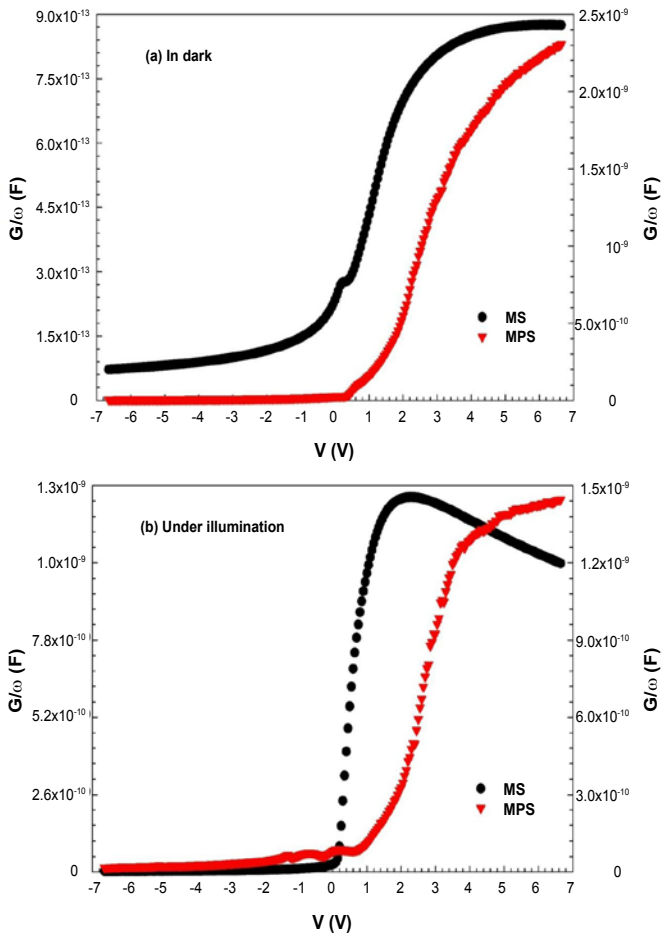

Figure 8: Measured conductance *G/ω* vs *V* of Au/n-Si SBD (MS) and Au/PVA (Bi-doped)/n-Si (MPS) type SBDs (a) in dark and (b) under illumination conditions.

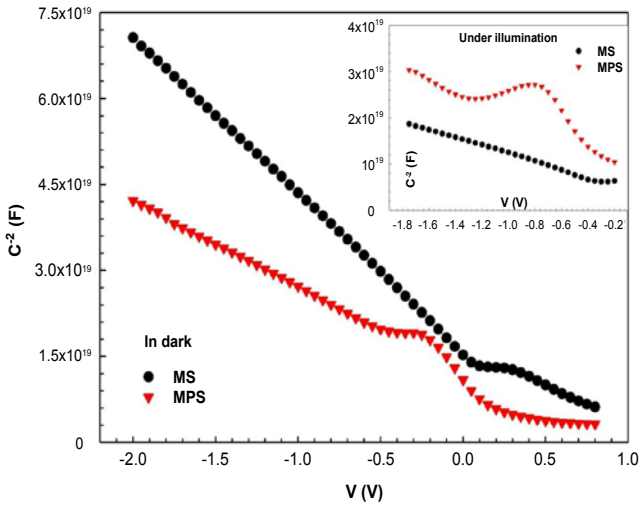

Figure 9: The reverse bias C^{-2}-V characteristics of MS and MPS type SBDs in dark and under illumination conditions.

IN DARK							
	V_o (V)	N_D (cm^{-3})	E_F (eV)	$\Delta\phi_B$ (eV)	W_D (cm)	ϕ_B (eV)	E_m (V/cm)
MS	0.608	4.48×10^{14}	0.27	0.010971	1.44×10^{-4}	0.892	9.866×10^{3}
MPS	0.802	8.07×10^{14}	0.26	0.0135	1.18×10^{-4}	1.073	1.459×10^{4}
UNDER ILLUMINATION							
	V_o (V)	N_D (cm^{-3})	E_F (eV)	$\Delta\phi_B$ (eV)	W_D (cm)	ϕ_B (eV)	E_m (V/cm)
MS	0.541	1.49×10^{15}	0.25	0.013855	6.88×10^{-5}	0.798	1.57×10^{4}
MPS	0.328	8.67×10^{14}	0.26	0.010676	7.03×10^{-5}	0.602	9.34×10^{3}

Table 2: The obtained V_o, N_D, E_F, W_D , E_m , $\Delta\phi_B$ and ϕ_B(C-V) values for MS and MPS type SBDs in dark, and under illumination conditions at room temperature, and 1MHz.

This discrepancy in BHs can be explained due to an interfacial layer or interfacial states in the semiconductor, the effect of image force lowering, barrier inhomogeneities and nature of measurement system [15,16,23-26]. Similar results have been reported in the literature for MS and MIS/MPS types SBDs in dark and illumination condition [28-32].

Conclusion

Forward and reverse bias *I-V*, *C-V* and *G/ω-V* characteristics of the fabricated MS (Au/n-Si) and MPS (Au/PVA (Bi-doped)/n-Si) were investigated in dark and under 200 W illumination intensity at room temperature. We aimed to prevent the reaction and inter-diffusion between the metal (Au) and semiconductor (n-Si), as well as to passivate active dangling bands at semiconductor surface, and so reduce the leakage current and N_{ss} density to improve the diode quality. Experimental results showed that the main electrical parameters, such as n, ϕ_b, R_s, R_{sh} and N_{ss} are strong functions of illumination level and applied bias voltage. The resistivity values were determined from the I-V characteristics by using Ohm's law. The energy distribution profile of N_{ss} was also obtained from the forward bias I-V characteristics, by taking into account voltage dependent n(V) and ϕ_e. In addition, the values of V_o, N_D, E_F, W_D, E_m, $\Delta\phi_B$ and ϕ_B*(C-V)* values for MS and MPS type SBDs were obtained from reverse bias C-V characteristics and compared. This discrepancy in BHs obtained from the forward bias I-V and reverse bias C-V was explained by an interfacial layer or interface states in the semiconductor, the effect of image force

lowering, barrier in homogeneities and nature of measurement system. It can be concluded that the Bi-doped interfacial PVA layer leads to considerable improvements in the diode performance, both in dark and under illumination conditions.

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